third and fifth peak doping concentrations are each at least 10 times greater than the second peak doping concentration and at least 10 times greater than the fourth peak doping concentration; a conductive control gate adjacent to the second, third, and fourth semiconductor layers; and a tunnel dielectric between the conductive control gate and the second, third, and fourth semiconductor layers.

[0212] One embodiment includes a non-volatile storage system, comprising a semiconductor substrate having a major surface; a three dimensional memory array of memory cells above the semiconductor substrate; a plurality of word lines coupled to the memory cells; a plurality of global bit lines; a plurality of vertically oriented bit lines electrically connected to the memory cells; and a plurality of vertically oriented thin film transistor (TFT) select devices that are above the semiconductor substrate, wherein the vertically oriented TFT select devices reside between the vertically oriented bit lines and the global bit lines. Each of the vertically oriented TFT select devices comprises a source having a first type of conductivity, wherein the source is electrically connected to a first of the global bit lines; a drain having the first type of conductivity, wherein the drain is electrically connected to a first of the vertical bit lines; a body between the source and the drain, wherein the body comprises a first region having a second type of conductivity that is opposite first type of conductivity, a second region having the first type of conductivity, and a third region having the second type of conductivity, wherein the second region is between the first region and the third region, wherein a peak doping concentration of the second region is greater than a peak doping concentration of the first region and is greater than a peak doping concentration of the third region, wherein the source, the body, and the drain are aligned with each other vertically with respect to the major surface of the substrate; and a control gate adjacent to the body.

[0213] The foregoing detailed description has been presented for purposes of illustration and description. It is not intended to be exhaustive or limiting to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the disclosed technology and its practical application, to thereby enable others skilled in the art to best utilize the technology in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope be defined by the claims appended hereto.

1. A semiconductor device, comprising:
a substrate having a major surface;
a first conductive region;
a second conductive region;
a thin film transistor comprising:
i) a first source/drain having a first type of conductivity, wherein the first source/drain is electrically connected to the first conductive region;
ii) a second source/drain having the first type of conductivity, wherein the second source/drain is electrically connected to the second conductive region;
iii) a body between the first source/drain and the second source/drain, wherein the body comprises a first body region having a second type of conductivity that is opposite first type of conductivity, a second body region having the first type of conductivity, and a third body region having the second type of conductivity, wherein the second body region is between the first body region and the third body region, wherein the second body region has a thickness as measured between the first body region and the third body region in the range between 50 to 120 nanometers, wherein a peak doping concentration of the second body region is greater than a peak doping concentration of the first body region and is greater than a peak doping concentration of the third body region, wherein the first source/drain, the body, and the second source/drain are aligned with each other vertically with respect to the major surface of the substrate; and;
iv) a control gate adjacent to the body; and
a management circuit coupled to the control gate, wherein the management circuit is configured to apply a first signal to the control gate to electrically connect the first conductive region to the second conductive region and to apply a second signal to the control gate to electrically disconnect the first conductive region from the second conductive region.

2. The semiconductor device of claim **1**, wherein the first body region and the third body region are p−, wherein the second body region is n+, wherein the first source/drain is n+ and wherein the second source/drain is n+.

3. (canceled)

4. The semiconductor device of claim **1**, wherein the first body region and the third body region are n−, wherein the second body region is p+.

5. The semiconductor device of claim **1**, wherein the second conductive region is a bit line that is oriented vertically with respect to the major surface of the substrate, wherein the first conductive region is a global bit line.

6. (canceled)

7. The semiconductor device of claim **1**, further comprising:
a plurality of non-volatile memory cells in a three-dimensional memory array, wherein the second conductive region is electrically connected to the plurality of non-volatile memory cells.

8-14. (canceled)

15. A semiconductor device, comprising:
a semiconductor substrate having a major surface that extends in a horizontal plane;
a first conductive line;
a second conductive line that extends in a vertical direction with respect to the horizontal plane;
a thin film transistor comprising:
a) a first semiconductor layer having a first peak doping concentration of a first type of conductivity, wherein the first semiconductor layer is electrically connected to the first conductive line;
b) a second semiconductor layer having a second peak doping concentration of a second type of conductivity that is opposite the first type of conductivity;
c) a third semiconductor layer having a third peak doping concentration of the first type of conductivity, wherein the third semiconductor layer has a thickness of between 50 to 120 nanometers;
d) a fourth semiconductor layer having a fourth peak doping concentration of the second type of conductivity;
e) a fifth semiconductor layer having a fifth peak doping concentration of the first type of conductivity, wherein the fifth semiconductor layer is electrically connected